

With respect to independent claims 1 and 7, which are similar in form, the Office Action maintains that Shinada discloses everything except for a data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock. Yet, as applicant has previously pointed out, Shinada's recording/reproducing apparatus stops its recording function temporarily if the audio data stored in the memory falls below a prescribed value, as illustrated in Fig. 1 and described at lines 6-23 of col. 6 of Shinada. This aspect of Shinada differs from the present invention which suspends the operation of the data processing circuit until the data stored in the buffer memory reaches a predetermined value. Moreover, Shinada stops the recording function for better data continuity, and does not describe or suggest suspending a data processing circuit by interrupting the power supply or by withholding the operation clocks applied to the data processing circuit, thereby reducing power consumption during operation. Still further, Shinada does not describe or suggest synchronizing the new data to be recorded onto the disk with the last recorded data immediately before the discontinuation of data recording, thereby assuring that the new data would be recorded in a region successive without break to the region with less recording data is recorded.

While these features, which are set forth in the claims in their present form, are not disclosed or suggested by Shinada, the Office Action does concede that Shinada does not disclose the feature of the data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by

halting the supply of an operation clock. For such features, the newly cited Landry reference is relied upon. Reference is made to lines 19-40 of col. 2 and lines 13-61 of col. 16 of Landry. The passages referred to describe halting of a system clock in which master processors write onto a host bus and slave processors write data to a buffer on a respective CPU board. Such data is compared with data on the host bus, and if not identical, the system clock is halted.

Consequently, Landry teaches halting of a system clock, but in a different type of system and for totally different reasons than in the case of the present invention. In the present invention, the data processing circuit for recording data is placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock until an amount of received data equivalent to a predetermined writing capacity has been stored in a buffer memory. This prevents data writing being performed intermittently so as to cause a waste of power. In Landry, the clock is stopped when data written to a buffer by slave processors is not identical to data written onto a host bus by master processors, in a system for operating tightly coupled mirrored processors in a computer system. That being the case, there is no teaching or suggestion in Landry that would lead one skilled in the art to modify Shinada so as to arrive at the claimed subject matter. Moreover, even if there were a basis for modifying Shinada based on the teachings of Landry, this would not overcome the further differences between Shinada and the present invention as claimed, as noted above. Therefore, claims 1-12 are submitted to clearly distinguish patentably over the attempted combination of references.

In conclusion, claims 1-12 are submitted to be allowable for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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